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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,100	09/09/2003	Tina J. Wagner	FIS920030249US1	2099
32074	7590	01/31/2006	EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION			VU, DAVID	
DEPT. 18G			ART UNIT	PAPER NUMBER
BLDG. 300-482				2818
2070 ROUTE 52				
HOPEWELL JUNCTION, NY 12533				

DATE MAILED: 01/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/605,100	WAGNER ET AL.
	Examiner	Art Unit
	DAVID VU	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 December 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 21-30,32,34,35,37,39 and 40 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 21-30,32,34,35,37,39 and 40 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 03/29/05 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.914

1. A request for continued examination under 37 CFR 1.114, including the, fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 07, 2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 21-30, 32, 34, 35, 37, 39 and 40 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Gilton (US Pat. 6,143,611) in view of Chang et al. (US Pat. 6,030,863, herein after Chang).

Gilton discloses in figs. 5-7 a SOI MOSFET device (col. 1, lines 24-28) comprising: a substrate 32 with a top substrate surface upon which a gate electrode stack is formed; gate electrode stack (col. 3, line 62 through col. 4, line 1) comprising: a polysilicon gate electrode 34 formed over a gate dielectric layer 33, gate dielectric layer 33 being formed on top substrate surface 32; polysilicon gate electrode 34 having a top gate electrode surface and having gate electrode sidewalls; sidewall spacers 50 formed on gate electrode sidewalls aside from gate electrode 34; a cap layer 35 having outer edges and a top formed on top gate electrode surface; a hard mask 39 formed on top of cap 35; notches formed in outer edges of cap layer 35 recessed from gate electrode sidewalls; notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of gate electrode layer 34 (col. 5, lines 11-33); and sidewall spacers 50 reaching along polysilicon gate electrode sidewalls to above a level at which protective plugs 50 contact gate electrode 34 whereby sidewall spacers 50 are contiguous with and overlapping protective plugs 50 covering sidewalls of polysilicon gate electrode 33 and a raised source/drain region 62/64 on top of said silicon layer 32 aside from spacers 50 (col. 5, lines 42-47).

Gilton discloses the gate electrode comprising a polysilicon gate electrode 34 and a cap layer 35 having a notches formed in outer edges of cap layer 35 recessed from gate electrode

sidewalls but fails to disclose the cap layer is an implanted amorphous silicon layer formed of germanium and silicon ions. However, Chang teaches amorphous silicon/ implanted amorphous silicon-germanium 60/polysilicon layer 20 is used for the gate electrode material (fig. 4 and col. 5, lines 12-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device/the gate structure of Gilton by using the gate electrode material as taught by Chang, in order to increase the conductivity of the gate electrode (See Abstract). Noted that the process of forming polysilicon/amorphous cap layer of Chang (fig. 4 and col. 5, lines 12-20) and that of the claimed invention is very much the same (see Specification [0028]).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DAVID VU
PRIMARY EXAMINER